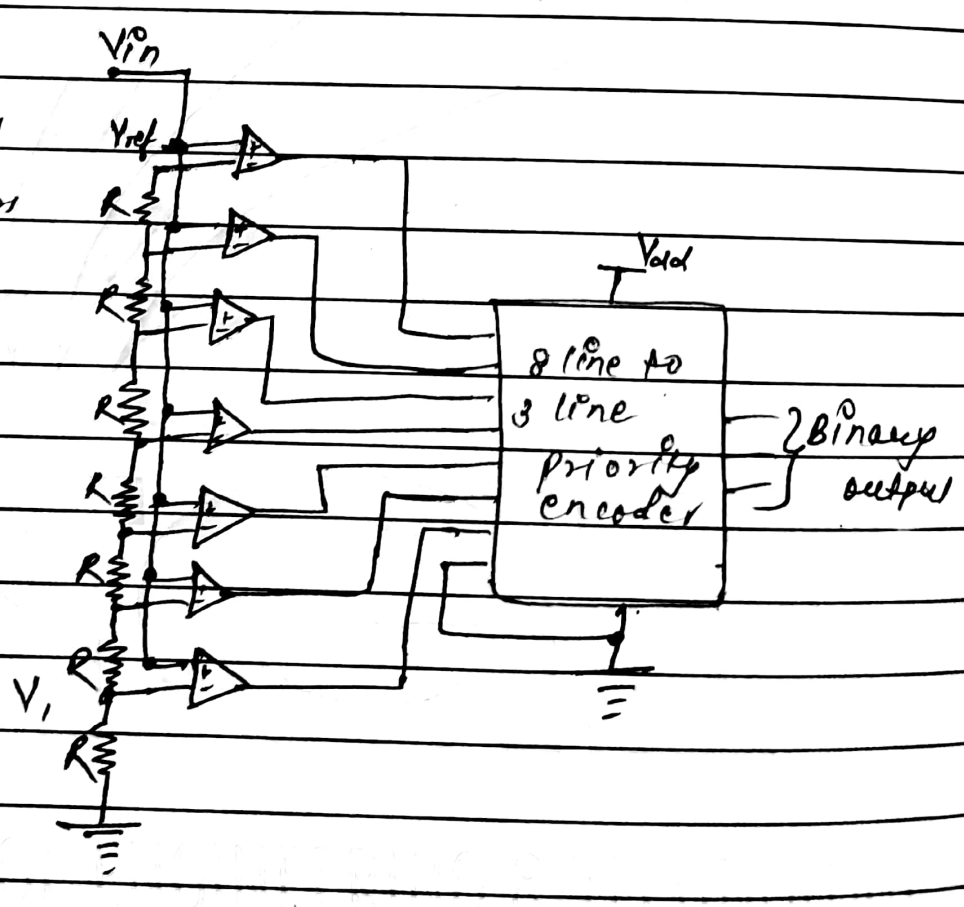
A/D converter

© Simultaneous A/D converter
- Parallel A/D converter
- flash ADC
- fastest among all other ADCs
- It consists of the high-speed comparator, the resistive voltage divider circuit and the encoder

- $(2^N - 1)$ Comparators
- 2^N Matched Registors
- Priority Encoder



- The input voltage is applied to the +ve terminal of the comparators.
- And through the voltage divider circuit, the

reference voltage is applied to the -ve terminal.
- A priority encoder is used to transform the comparator outputs to the correct digital binary output.

If V_1 is the voltage to the first comparator Then this V_1 can be given by;

$$V_1 = \left(\frac{R}{R+7R} \times V_{ref}\right)$$

$$\boxed{V_1 = \left(\frac{V_{ref}}{8}\right)}$$

- If V_2 is the second voltage to the 2nd Comparator, Then

$$V_2 = \left(\frac{R+R}{R+7R} \times V_{ref}\right)$$

$$\boxed{V_2 = \left(\frac{2\,V_{ref}}{8}\right)}$$

So, as we go forward, $\boxed{V_7 = \frac{7\,V_{ref}}{8}}$

Signature of Immediate Reporting Officer

Name

Signature of Student

Designation

THIRD FORTNIGHT PROGRESS REPORT

Date : Let $V_{ref} = 8V$, $V_{in} = 3.3V$

$$V_1 = \frac{V_{ref}}{8}$$

$$V_1 = \left(\frac{8}{8}\right) = 1V$$

Similarly, $V_2 = 2V$, $V_3 = 3V$ . . . . . $V_7 = 7V$

By Priority Encoder, we will get output from 3rd comparator.

= 1 1 1 0 0 0

(1V) (2V) (3V) (4V) (5V) (6V) (7V)

Advantages :- ① fastest ADC

② Suitable for large bandwidth applications such as satellite comm^n, radar processing and fast data acquisition for the Oscilloscope.

Disadvantages :- ① High power consumption.

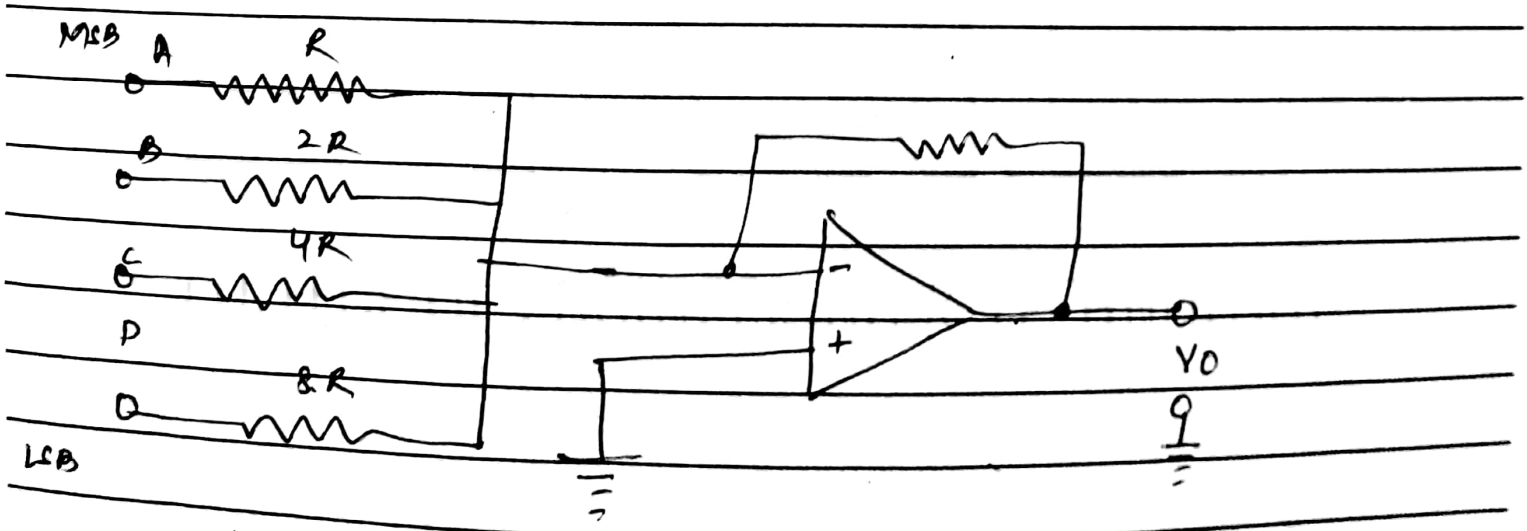
② Limited resolution (typically up to 8 bits)

- large die area ($2^N - 1$) comparators
- Component Matching (resistors & comparators)

Weighted Resistor D/A converter

This is a simple method where each bit signal is connected with weighted resistor.

- The MSB input is connected with lowest resistor and as we move forward towards to LSB the resistance value is made twice of previous resistor.
- The purpose of increasing the resistor value is to pass minimum current through LSB resistance called Max current through MSB resistance.
- The network connected in this method is also known as "Variable Resistor Network"



4 bit weightage Resistor D/A converter with OPAMP

- Here we using summing amplifier is used.
- four digital Inputs A, B, C, D.
- The input to the ckt can be connected by using four switches (SPDT) so that each switch can be either at 0 level or 1 level.

The output voltage of the D/A converter is given by

$$V_{out} = -R_f \left(\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} + \frac{V_d}{R_d} \right) \quad \text{.... Summing Amplifier}$$

In this ckt, $R_f = R$ so.

$$V_o = -R \left(\frac{A}{R} + \frac{B}{2R} + \frac{C}{4R} + \frac{D}{8R} \right)$$

Incomplete

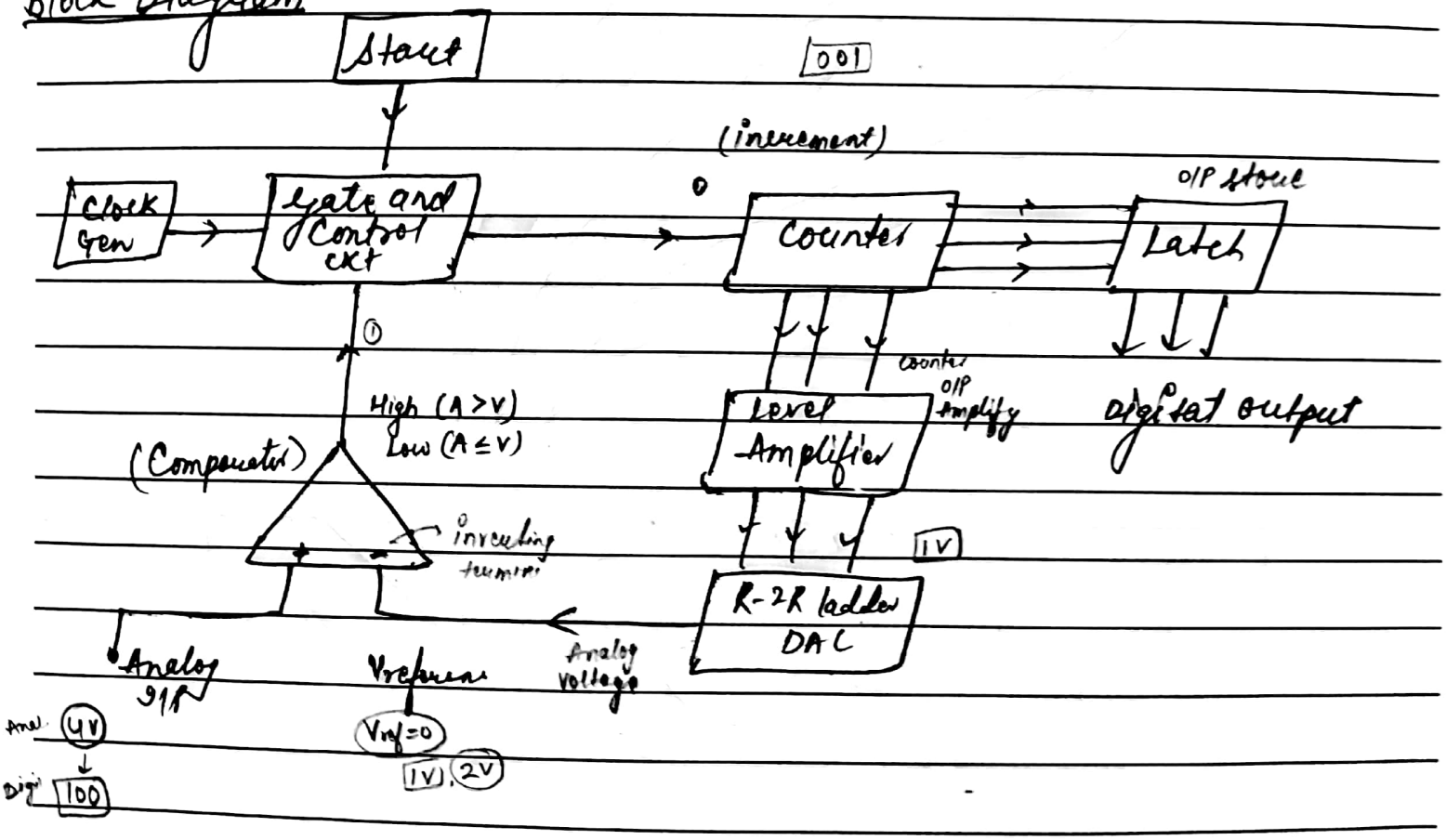
↓

continuous in nature

② Counter type A/D converter :-

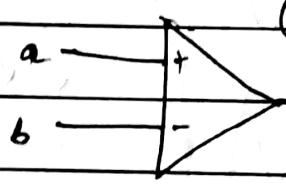
Definition :- A counter type ADC produces a digital output which is approximately equal to analog input by using counter operation internally.

Block Diagram



The block Diagram of counter type ADC is shown above and it consist of following main blocks -

① Comparator :- When OPAMP is used in open loop configuration then it can be used as comparator.
The output of the comparator will be high (or 1) as long as the voltage at non-inverting terminal is greater than the inverting terminal and output will be low (or 0) as long as the voltage at non-inverting terminal is less than or equal to the voltage at inverting terminal.



(If $a > b$, V_o = High)
V_o
(If $a \leq b$, V_o = Low or zero)

② clock signal generator - It generate the clock pulses

→ clock Pulse.

③ Control Logic - The control logic resets the counter and enables the clock signal generator to send the clock pulses to the counter, when it received the start commanding signal.

Signature of Immediate Reporting Officer

Name

Signature of Student

Designation

FOURTH FORTNIGHT PROGRESS REPORT

Date : ④ counter → The counter gets incremented by one for every clock pulse and its value will be in digital format. The output of the counter is applied to DAC.

⑤ DAC - DAC converts the received digital input into an analog output.
The DAC used may be of binary weighted resistor type or R-2R / ladder type.

⑥ Latch - Latch is used to store the output of counter.

Working of counter type ADC :-

To understand the working, let the analog input is 4V, which is to be converted into its binary equivalent digit.
Let in the beginning the reference voltage, V_{ref} is zero. So at the non inverting terminal of comparator is 4V which is greater than the voltage at inverting terminal (i.e 0V. So the comparator gives high output. As soon as this high output reaches to gate and control signal ckt, it enables the

the clock generator to send the clock pulse to the counter, when control signal receives the start command.

So the counter gets increment by one i.e output of the counter becomes 001 and this output is then send to level amplifier. At the same time this output is send to latch which stores this output. Now this output of counter i.e 001 serves as input of DAC.

This DAC converts it into equivalent digital input i.e 1V. This 1V is send to inverting terminal of comparator.

Again 4V>1V, so counter gets incremented and the output of DAC now becomes 2V.
Again 4V>2V, the counter again gets incremented by 1 and the o/p of DAC becomes 3V.

Once More 4V>3V, the counter gets increment by 1 and the o/p of counter becomes 100 which is equivalent to 4V. and the same output is send to DAC which in turn is send to comparator.

Now the voltage at the inverting & non-inverting terminal of the comparator becomes equal and this gives low output.

Now, the clock generator does not send any clock pulse to the counter and the output of counter remains 100 which gets stored in the latch and thus 4V analog input gets converted into its binary equivalent 100.

In this way an analog input can be converted into its binary equivalent.

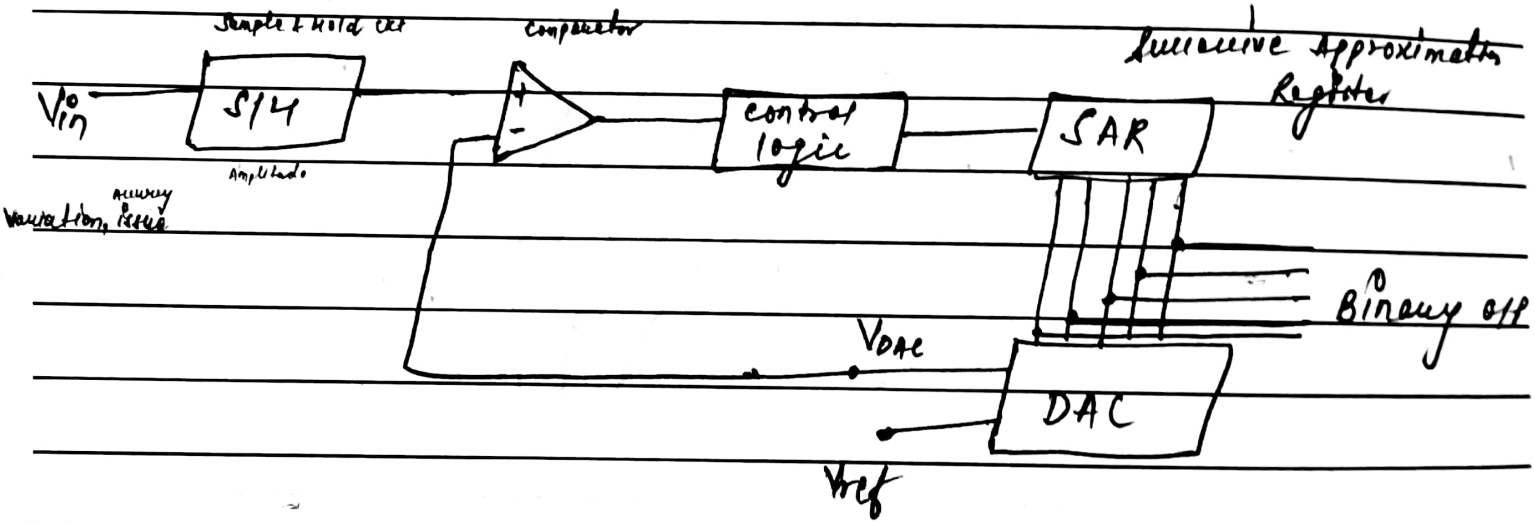
The only disadvantage of this type of ADC is that it requires the same no. of clock pulses equal to the analog input voltage.

for example- To convert 4V into binary no, we require 4 no. of clock pulses.

Successive Approximation ADC

- It has low conversion time.
- Most commonly used ADC
- Use in general purpose Applications.

Circuit Diagram:



SAR :- Every time gives positional MSB → 1 or 0

- If $V_{in} > V_{DAC}$
  or output of comparator = 1
  Next MSB = 1
  Previous — = same 1
- If $V_{in} < V_{DAC}$ or
  o/p of com = 0
  Next MSB = 1
  Previous MSB = change 0

Working → let V_{in} = 13.2 volt

V_{ref} = 16 volt

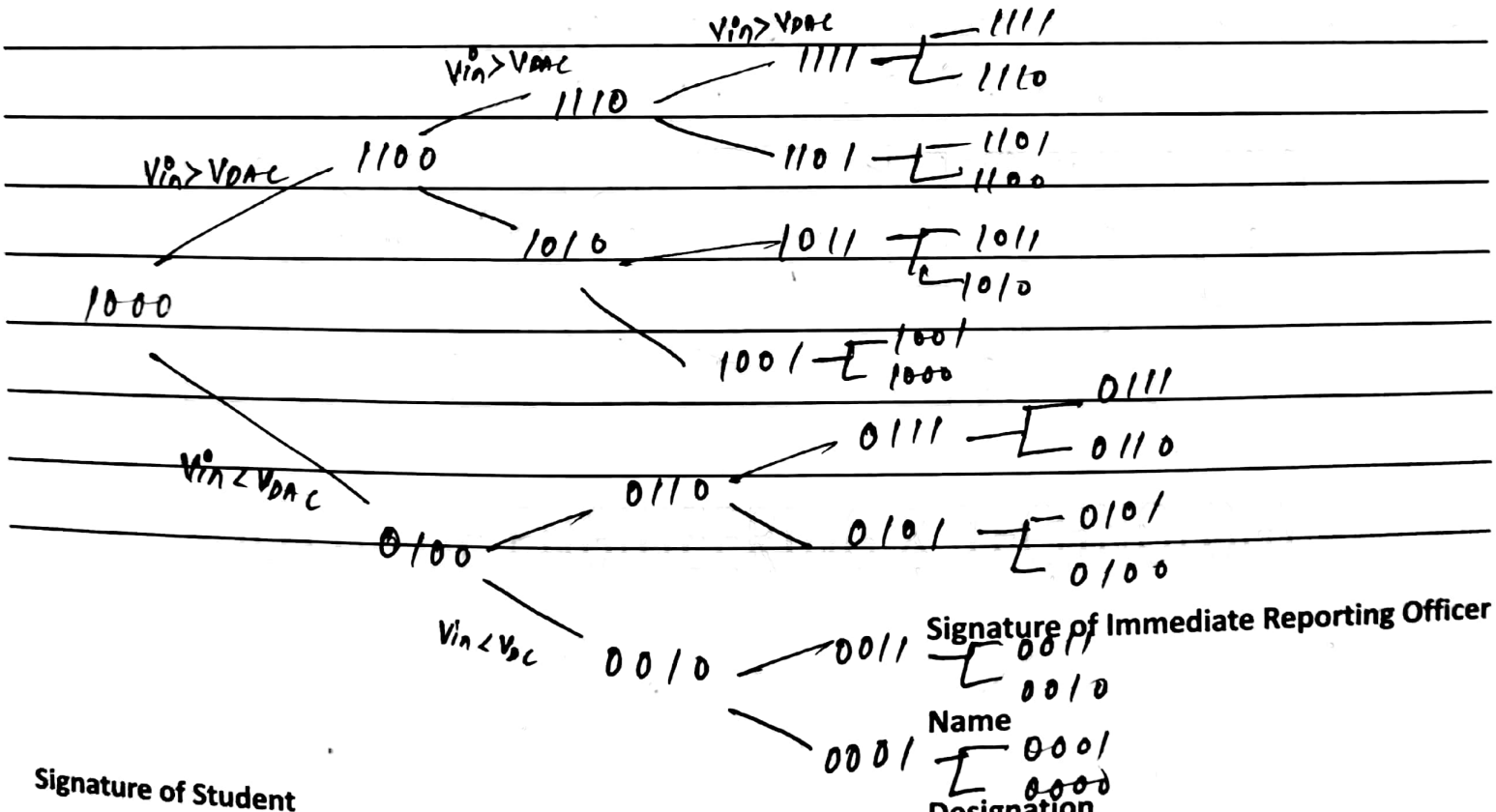
O/P of SAR = 1000

V_{DAC} = 8 Volt

output of comparator = 1

- V_{in} = 13.2 volt
  SAR = 1100
  V_{DAC} = 12 volt
  $V_{in} > V_{DAC}$
- V_{in} = 13.2 volt
  SAR → 1110
  V_{DAC} → 14 volt
  $V_{in} < V_{DAC}$
- V_{in} = 13.2 volt
  SAR = 1101
  V_{DAC} = 13 volt
  final output

Conversion time = N × T_{CL}



Signature of Immediate Reporting Officer

Name

Designation

Signature of Student

FIFTH FORTNIGHT PROGRESS REPORT

Date: Advantage -

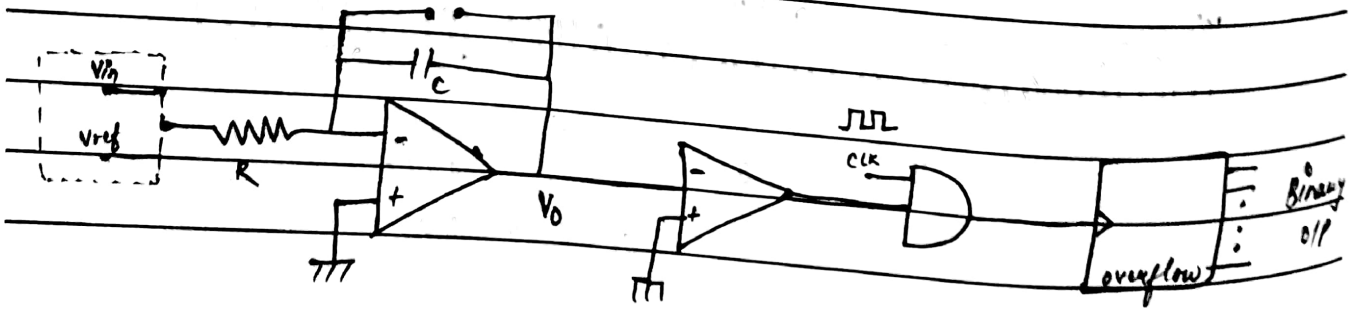
- low conversion time
- low latency time
- Independent of input voltage
- low power consumption
- High accuracy
- Easy to use

Dual slope ADC

- It eliminates the drawback of Single slope ADC
- It has high accuracy & Resolution & noise Immunity
- It takes more time for conversion.
- It has 3 components
  (i) Integrator (ii) comparator (iii) counter

Circuit Diagram :-

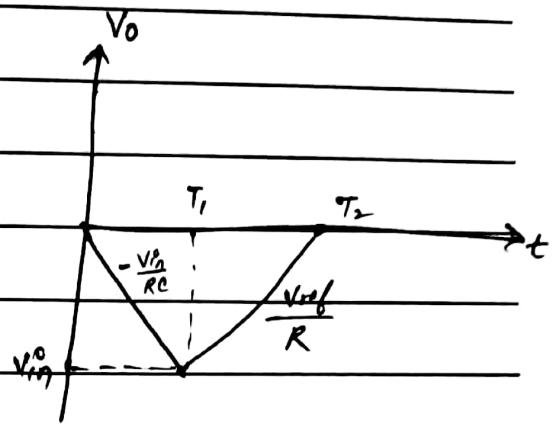
$$V_0 = -\frac{1}{RC}\int v\,dt$$



Working:-

Part① Integrator

$$V_o = \frac{-1}{RC}\int V_{in}\cdot dt$$



After time T_1

$$\boxed{V_o = \frac{-T_1 V_{in}}{RC}}$$

After $t = T_1$

Switch connects to $-V_{ref}$

$$V_o = \frac{-1}{RC}\int_0^{T_2}(-V_{ref})\,dt + V_{initial}$$

$$V_o = \frac{V_{ref}\cdot T_2}{RC} - \frac{T_1 V_{in}}{RC} = 0$$

at $t = T_2$, $V_o = 0$ $\Rightarrow$ $\frac{V_{ref} T_2}{RC} = \frac{T_1 V_{in}}{RC}$

$$\Rightarrow \boxed{T_2 = \frac{T_1 V_{in}}{V_{ref}}}$$

(V_{ref} fixed)

$$\boxed{T_2 \propto V_{in}}$$

Date

Expt. No. Page No.

Unit → 4

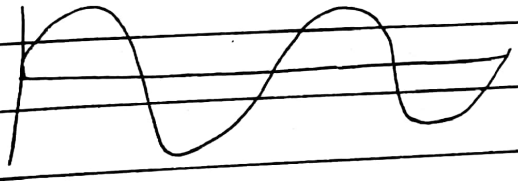
A/D and D/A Converters

Digital signal → 0, 1

Analog " → 1-10 (infinite range)

Analog An Analog Signal is continous in both time & amplitude

eg:- Sound Wave, Voltage range (0-5), temperature

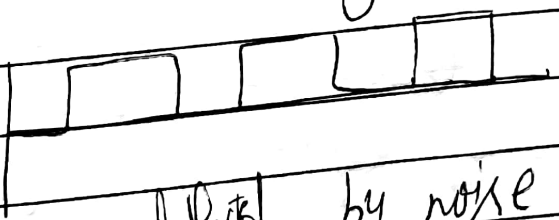


Digital A digital signal is discrete in both time & amplitude.

It can take only fixed values (0, 1)

eg:- Data in computer

digital Clocks



less affected by noise

(In analog (0 & 1) also occur but not stayed due to continuous & infinite possible values)

Teacher's Signature :

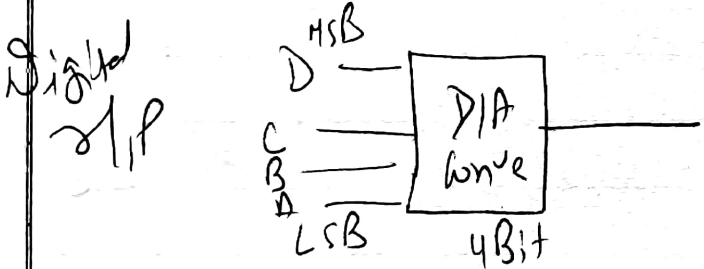
Basics of D/A & A/D Converter

D/A → The Process of Converting digital to Analog data is called Digital to Analog Conversion ; & that

It is Decoding device.

Two methods of D to A

1. Weighted register D/A Converter
2. R-2R ladder D/A "



$(2^4 = 16)$ Possible

A/D The process of converting Analog data to digital data is called Analog to digital convertor.

Types ;- Successive Approximation type

Date

Expt. No. Page No.

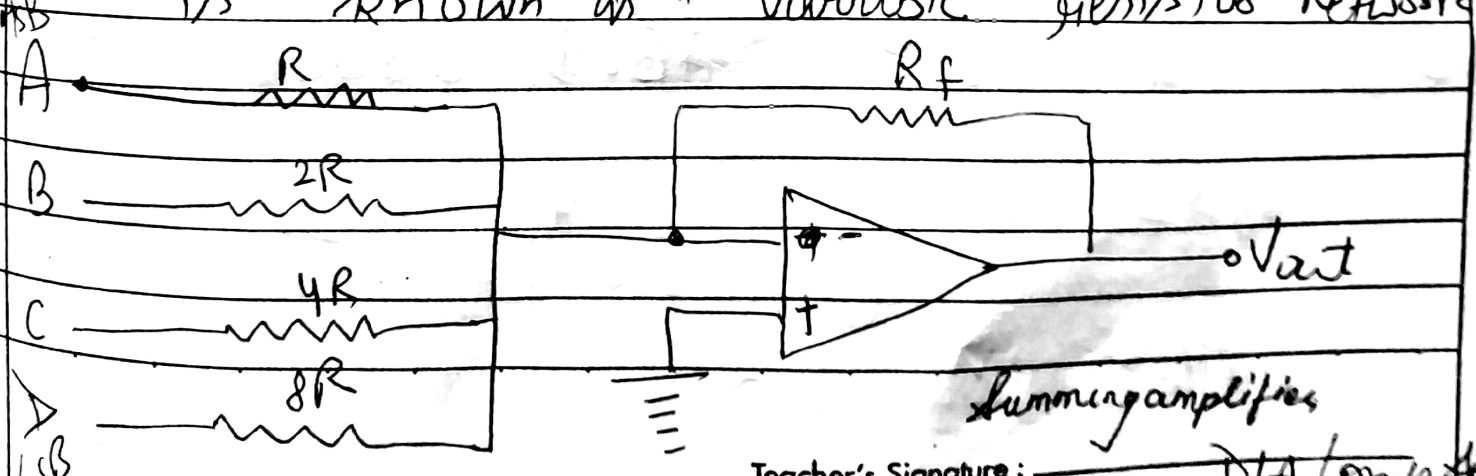
Weighted Resistor Converter (part of D to A)

This is a simple method where each bit signal is connected with weighted resistor.

The MSB I/P is connected with lowest resistor and as we move forward towards to LSB the resistance value is made twice of previous resistor.

The purpose of (↑)ng the value of resistor is to pass minimum current through LSB resistance while maximum current through MSB resistance.

The network connected in this method is known as "Variable resistor Network".



summing amplifier

4 Bit Weightage Resistor D/A converter with Ramp.

Teacher's Signature :

We know that for summing amplifier is used. So that Output voltage of D/A converter is

$$V_{out} = -R_f\left[\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} + \frac{V_d}{R_D}\right]$$

(i/p voltage)

Now
In this ckt $\boxed{R_f = R}$

$$\boxed{V_0 = -R\left[\frac{A}{R} + \frac{B}{2R} + \frac{C}{4R} + \frac{D}{8R}\right]} = -\left(\frac{V_3}{2^0} + \frac{V_2}{2^1} + \frac{V_1}{2^2} + \frac{V_0}{2^3}\right)$$

Put $R = 1$

$$V_0 = -\left[\frac{A}{2^0} + \frac{B}{2^1} + \frac{C}{2^2} + \frac{D}{2^3}\right]$$

→ n-bit inputs given

→ 8×1 I/p + o/p in 2 power form

Let take two voltage level

0 = 0 V
1 = 5 V

Case 1) When I/P ABCD = 0000

$$V_0 = -R\left(\frac{0}{R} + \frac{0}{2R} + \frac{0}{4R} + \frac{0}{8R}\right)$$

$\boxed{V_0 = 0V}$

Expt. No. _____ Date _____

Page No. _____

Case 2 When I/P ABCD = 0001

$$V_0 = -R\left[\frac{4}{8R}\right]$$

$$V_0 = \frac{-1}{2} = -0.5\ V$$

Case 3 → When I/P ABCD = 0010

$$V_0 = -1V$$

Case 4 → I/P ABCD = 0011

$$V_0 = -R\left[\frac{4}{4R} + \frac{4}{8R}\right]$$

$$= -R\left[\frac{2+1}{8R}\right] = -R\left[\frac{1}{R} + \frac{1}{2R}\right]$$

$$V_0 = -1.5V$$

Drawbacks - If we ↑ bit of DAC, accuracy reduced, produce distorted o/p.

1) Each resistor handles different value of current, so all have diff voltage.
2) MSB is resistor is required to handle large current.
3) Any changes in temp. will cause change in resistance, which will affect the o/p voltage.
4) To overcome these problem ex: R-2R developed.

Teacher's Signature : _____

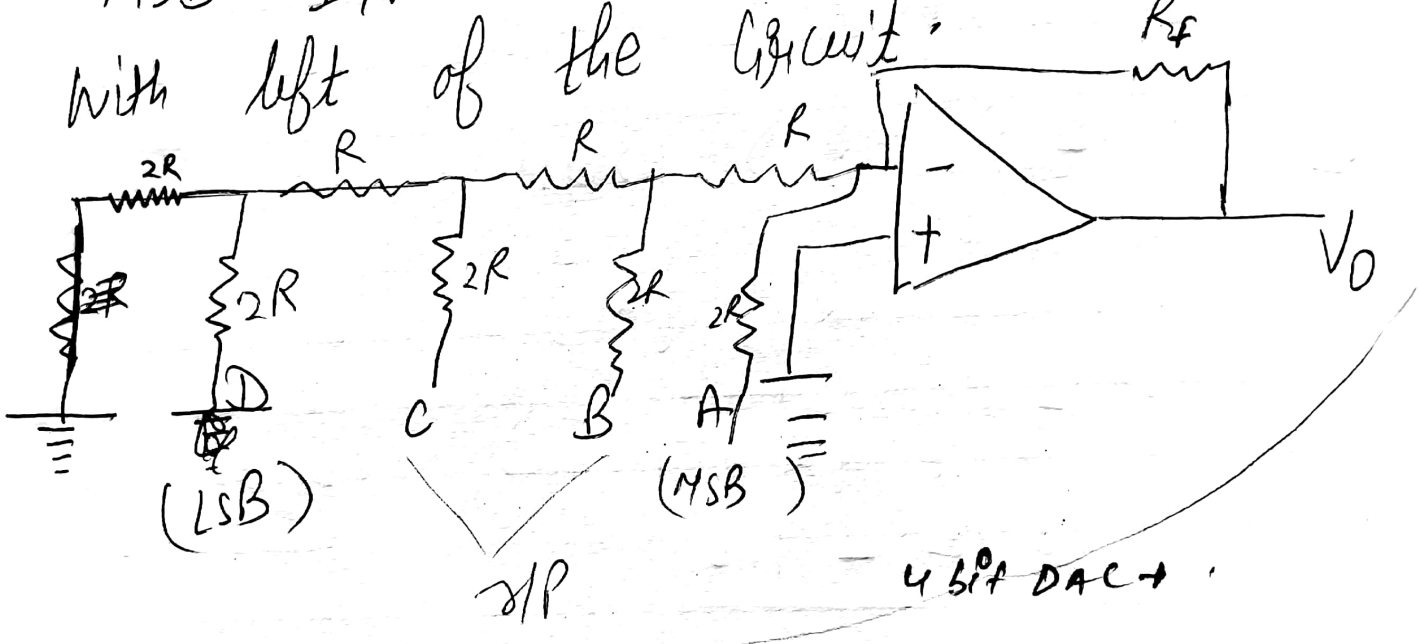
R-2R ladder D/A Converter

R-2R ladder is a resistive network, it contains only two resistor values

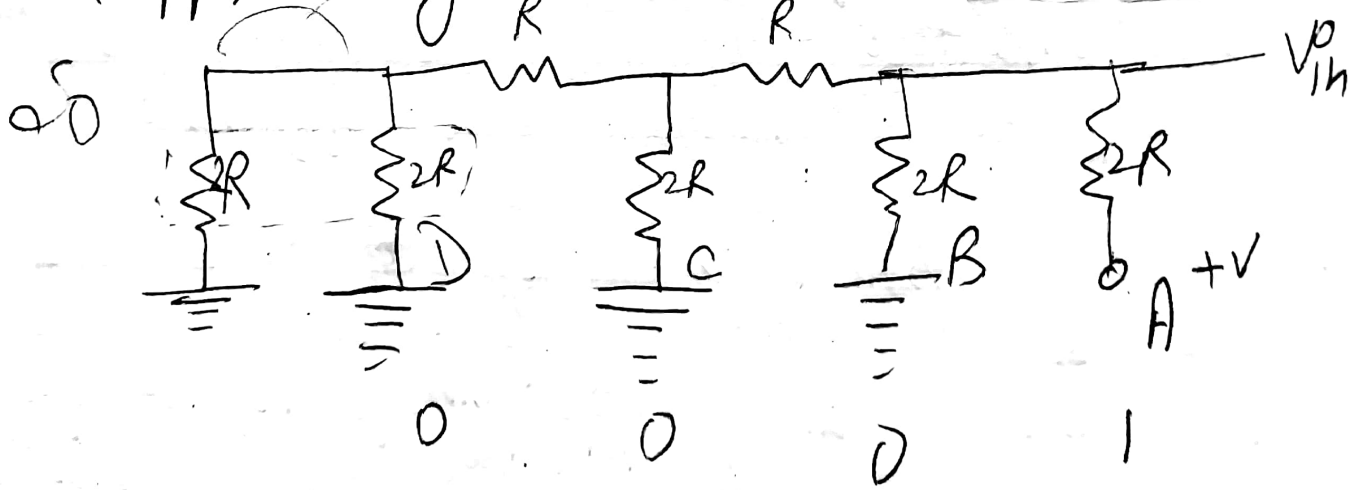
R & 2R.

It has op-amp as a scaling ckt.

MSB I/P towards right & LSB I/P with left of the Circuit.



Suppose digital I/P is ABCD = 1000



Date

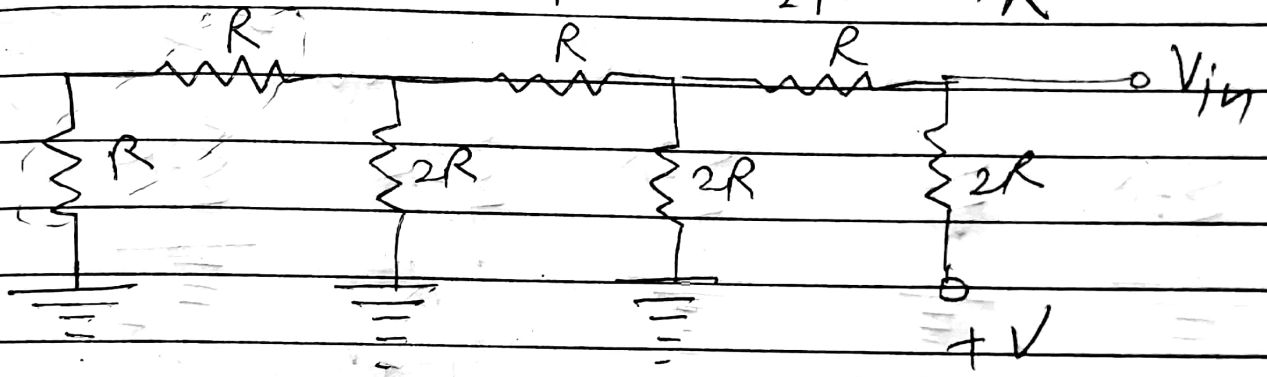
Expt. No. Page No.

BED will be grounded due to zero

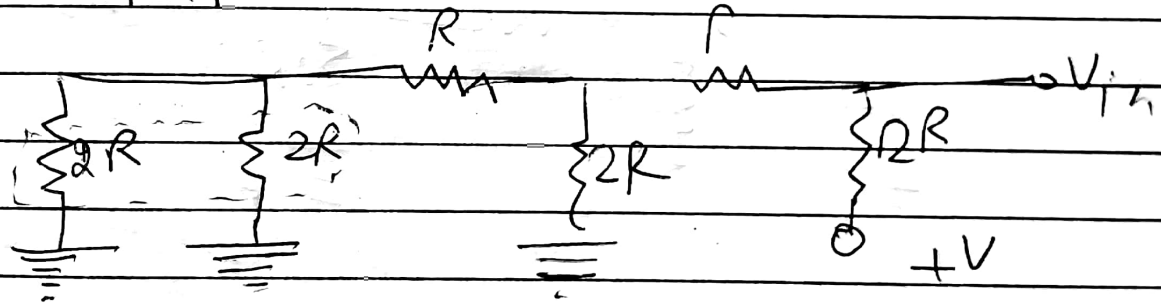
$2R \parallel 2R = R$

$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2}$

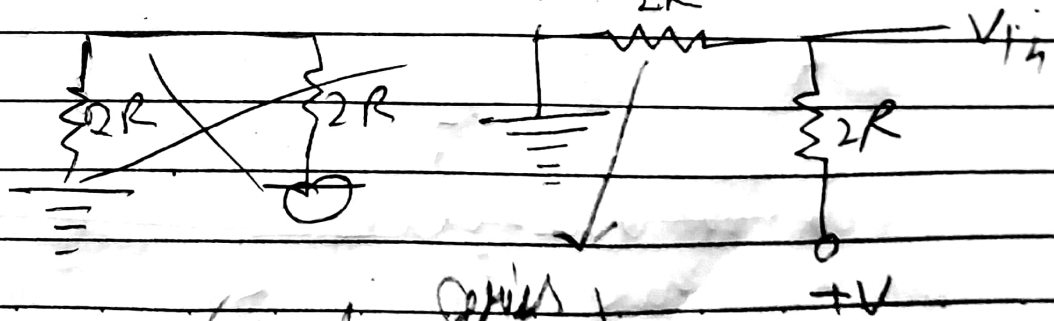
$= \frac{1}{2R} + \frac{1}{2R} = \frac{2}{2R} = \frac{1}{R}$



series $R+R = 2R$



Do the same process series & parallel we get



where (1) series

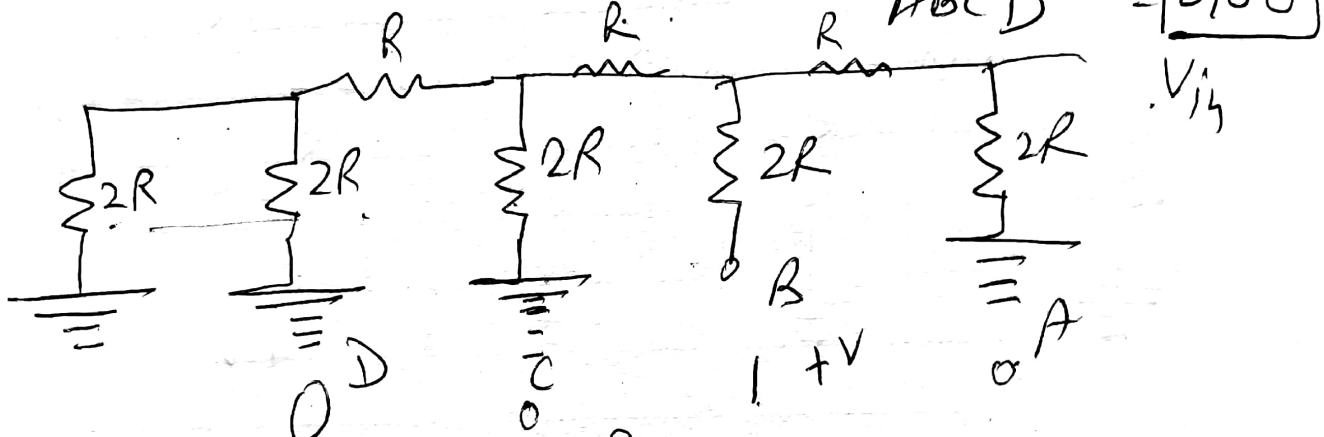
Teacher's Signature :

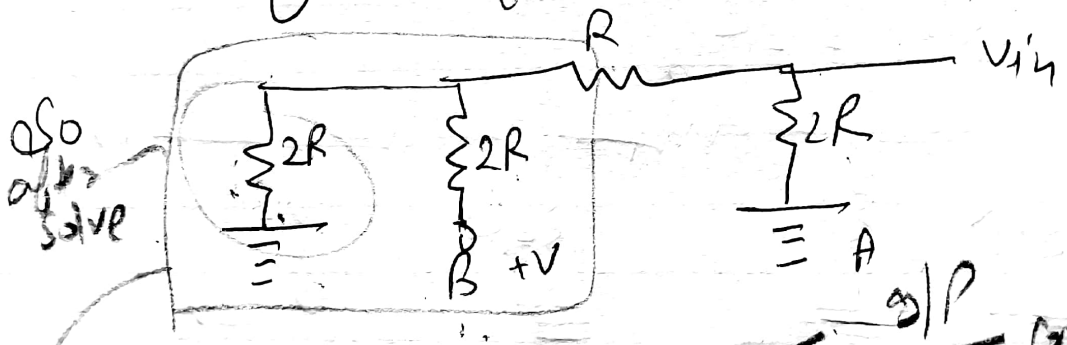
By voltage divider

$$V_{in} = \frac{V \times 2R}{2R + 2R} = \frac{V \times 2R}{4R} = V/2$$

when ABCD = 1000 then $V_{in} = V/2$

Now Another case suppose digital I/P ABCD = 0|00

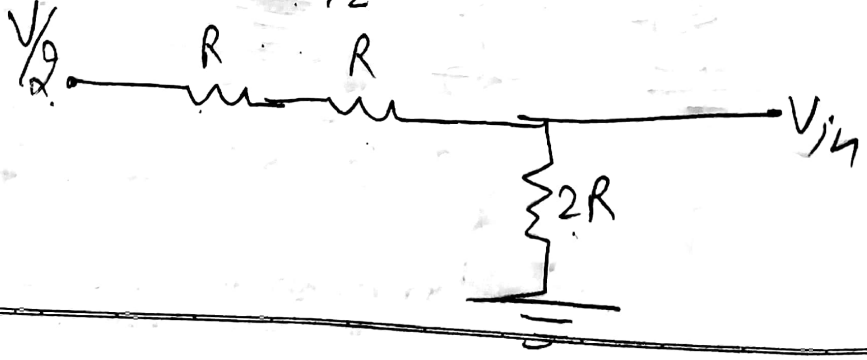




O/P connected to resistance

Voltage divide $V_{in} = \frac{V \times 2R}{4R}$ → Total resistance

$= V/2$



Expt. No. _____ Date _____

Page No. _____

By voltage divider

$$V_{in} = \frac{V \times 2R}{2 \times 4R} = V/4$$

=

when ABCD = 0010 then $V_{in} = V/8$

" ABCD = 0001 " $V_{in} = V/16$

" " = ~~V/2~~ = ~~V/8~~

The o/p D/A Converter can be Calculated by using summing amplifier eqⁿ.

$$V_0 = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{V_3} + \frac{V_4}{R_4} \right)$$

$$= -R_f \left(\frac{A}{2R} + \frac{B}{4R} + \frac{C}{8R} + \frac{D}{16} \right) V$$

$V_1 = A/2$, $V_2 = B/4$, $V_3 = C/8$, $V_4 = D/16$

$R_f = R$

$$V_0 = -\frac{R}{R} \left(\frac{A}{2} + \frac{B}{4} + \frac{C}{8} + \frac{D}{16} \right)$$

$$= -\left(\frac{A}{2^1} + \frac{B}{2^2} + \frac{C}{2^3} + \frac{D}{2^4} \right)$$

Teacher's Signature : _____

Explaining more

I/P	O/P
0000	0
0001	-0.625.
0010	-1.25.
0011	-1.875

Advantages

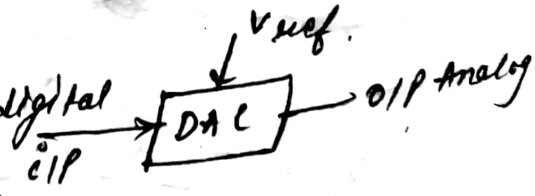
(1) Easier to built accurately as only 2 precision metal film resistor are required

(2) No. of bits can be expanded by adding more sections of same R/2R value.

(3) In inverted R/2R ladder DAC, node voltage remain const. with changing I/P binary words.

(4) This avoids any slow down effects by stray capacitances.

- It uses only two Resistors.
- It gives accurate O/P
- It can used for Higher no. of bits
- It has O/P impedance (R), will not affect other circuitry



Date

Expt. No. Page No.

Specifications for D/A Converters

Parameters used to describe the characteristics of D/A converters are.

① **Resolution:-** This is defined as the smallest possible change in the analog o/p as a result of a change in the digital I/P. This is also referred as Step Size and it is always equal to the weight of LSB.

For n-bit DAC

no. of possible steps or level $= 2^n - 1$

$$\text{Step size or Resolution} = \frac{\text{Full Scale O/P}}{\text{No. of Steps}}$$

$$= \frac{\text{Full Scale O/P}}{2^n - 1}$$

eg:- Full Scale Voltage = 10V

$n = 8$

$$\text{Step Size} = \frac{10}{2^8 - 1} = \frac{10}{256 - 1} = \frac{10}{255} \text{ V}$$

$$\therefore \%R = \frac{\text{Step Size}}{\text{Full Scale O/P}} \times 100 = \frac{\text{Full Scale O/P}/2^n - 1}{\text{Full Scale O/P}} \times 100$$

Teacher's Signature:

$$R = \frac{1}{2^n - 1} \times 100$$

(2) Accuracy :- how much error can be tolerate.

It is measure of the difference b/w the Actual o/p voltage & the expected o/p voltage. It is specified as a full scale or maximum o/p voltage.

eg :- VFS = 10V & accuracy = ± 0.2%.

max error = VFS × .2%.

$$VFS \times \frac{0.2}{100} = 10 \times \frac{.2}{100} = 0.02V$$

(3) Linearity → Linearity means if we do a small change ~~occurs~~ in I/P, as it is same change should be occur in o/p as well. But this is not possible ideally

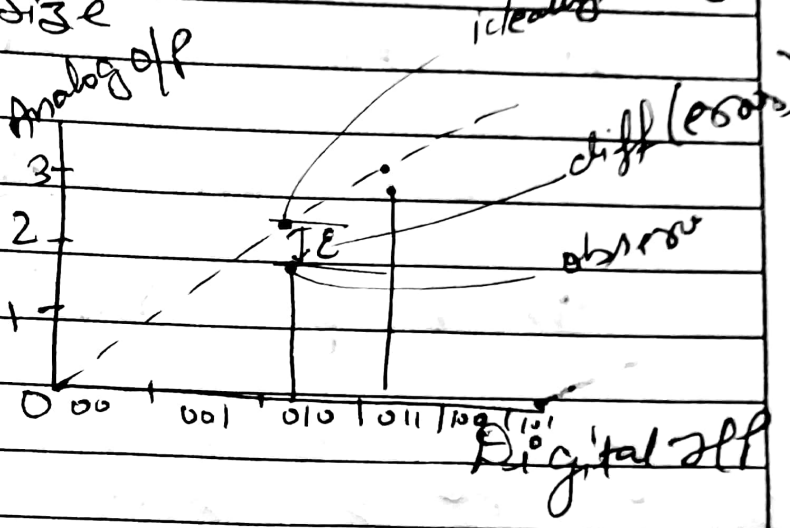
This error is max. deviation in step size from the ideal step size. This is indicated by E. The linearity of a

Date

Expt. No. Page No.

DAC is generally specified by comparing ε & Δ → step size

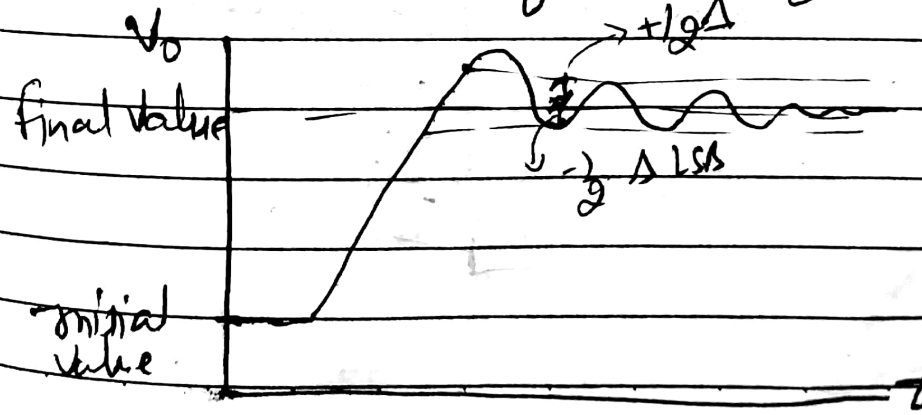
$$|\varepsilon| \leq \frac{1}{2}\Delta$$



(4) Settling Time :- Time required for DAC o/p to go from zero to full scale.

The operating speed of DAC is specified by Settling Time.

It is measured as the time for the ~~Scale~~ DAC o/p to settle with in $\pm\frac{1}{2}\Delta$ (step size) of its final value.

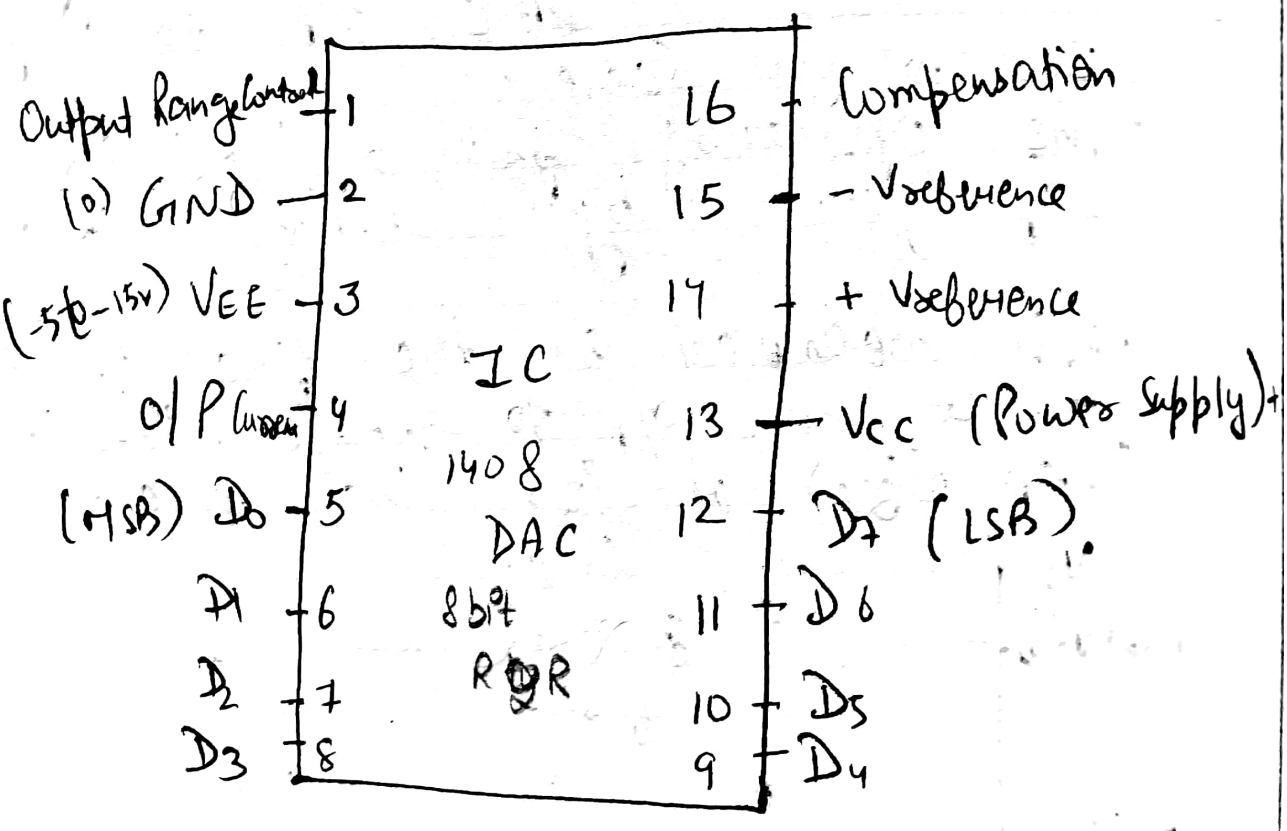


Teacher's Signature :

(5) Temperature sensitivity

The analog o/p varies with temp. for any fixed digital i/p change in o/p with temp is referred to as temp. sensitivity.

Example of D/A converter ICs



Date

Expt. No. _____ Page No. _____

It is a TTL IC, made up of CMOS.
8 Bit, R-2R network used in this

We can use 8 Bit here
It is dual in line IC (8-8 line (Total 16)

(5/12) $(D_0 - D_{12})$ - 8 Bit I/P

(Pin 14-15) apply reference Voltage in I/P

Pin 16 → Compensation

Pin 3 → V_{EE} Connect to Source (in npn & pnp

Pin 4 → We get Output here

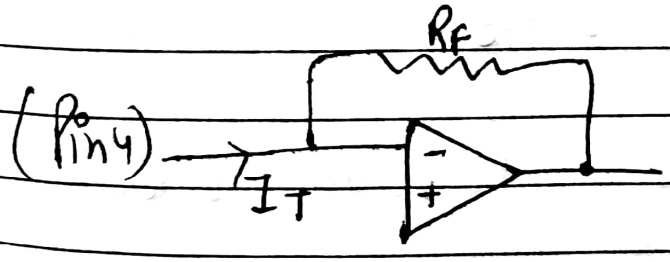
$$I_{out} = \frac{V_{ref}}{R}\left(\frac{D_0}{2} + \frac{D_1}{4} + \frac{D_2}{8} + \frac{D_3}{16} + \cdots \frac{D_7}{256}\right)$$

(acc to weightage)

R-2R ki find

We want Vout

So Connect R-2R to op amp & get O/P



IC 741

$= -1.992 \times 2.5\,k$

$V_0 = -4.98\ V$

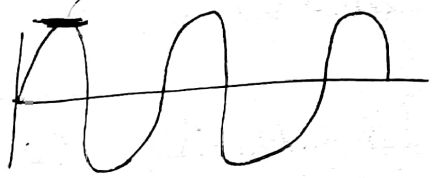
(If D_0 to $D_7 = 1$)
& $V_{ref} = +5\ V$
$R = 2.5\ V$

We get $I_0 = 1.992\ mA$

Teacher's Signature : _____

Sample & hold Circuit

The Sample & hold ckt is an electronic ckt which creates the voltage Sample given to it as i/p & after these it holds these samples for definite time.

Sample → 

i/p की 1/3 Part consider करता है Sample

Sampling Time → Time during which ckt generate Sample

Hold → Sample को particular time तक hold करके रखता है।

Holding Time:- Time during which ckt holds the sampled value is called holding time.

Sampling time → 1μsec to 14μsec

Holding time → not define, depend on application.

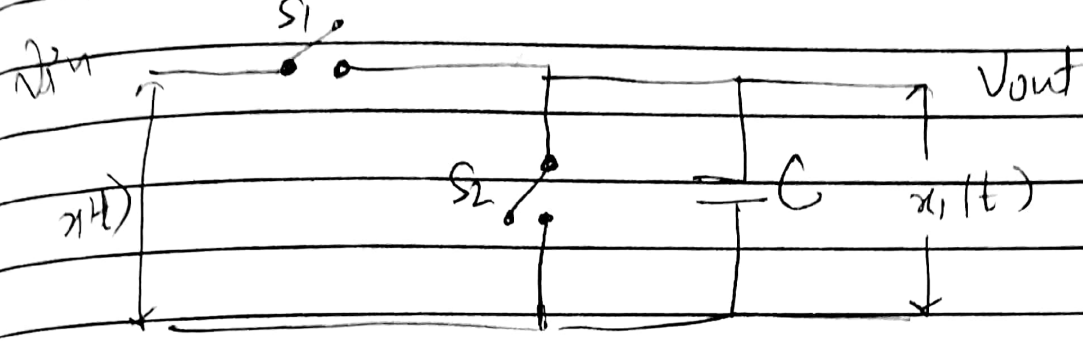
Time during which the ckt generate the sample of the input signal is called sampling time.

Date

Expt. No. _____ Page No. _____

Working

In this ckt only capacitor & Switch are used



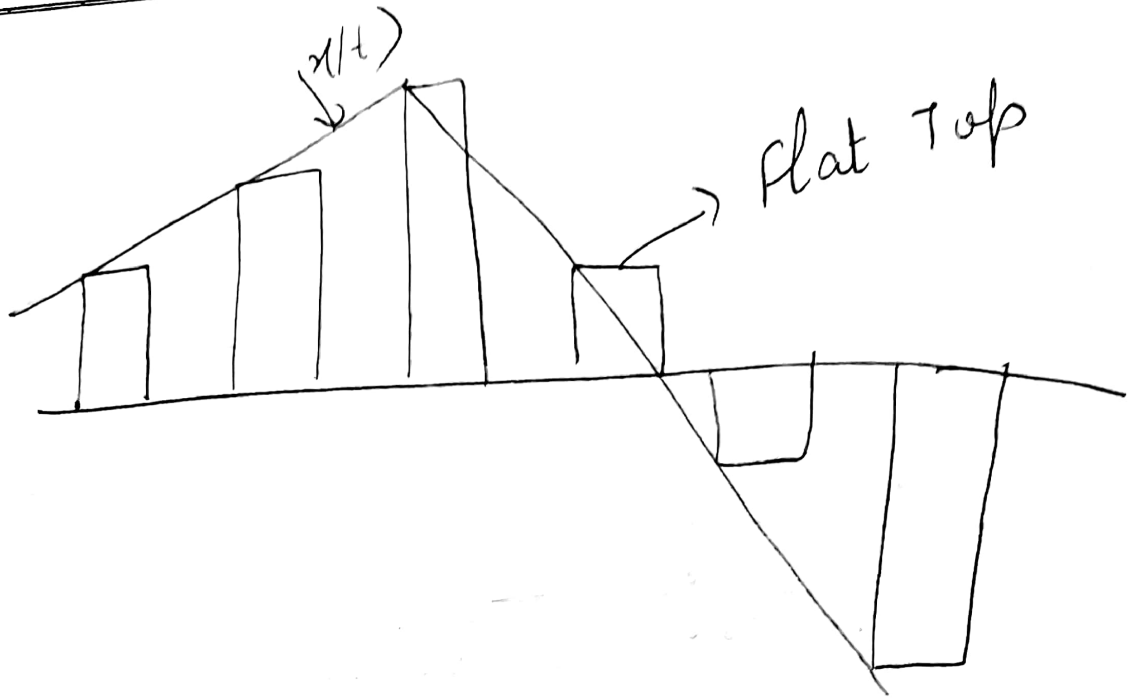
C is Sor heart of Sampled ckt

Switch S_1 is used as Sampling switch and S_2 is used as discharging ".

when S_1 → Closed for short duration C will get charged & upto its Peak value or a voltage equal to its instantenous Sample value of increasing Signal x(t).

Now S_1 → open & S_2 → closed C get discharge & has no voltage.

Teacher's Signature : _____



~~Used~~ Users

(1) To get flat top PAM (Pulse amplitude modulation)

(2) ckt Used when multiple samples need to be measured at same time. Also useful for remove variations in I/P signal.

(3) The purpose of this ckt is to sample an analog I/P signal & hold this value over a certain length of time for subsequent processing.

(4) In order that I/P voltage is held const for all practical purposes, it is essential that C has very low leakage.

Date

Page No.

Expt. No.

Analog To Digital Converters

Quantization & Encoding

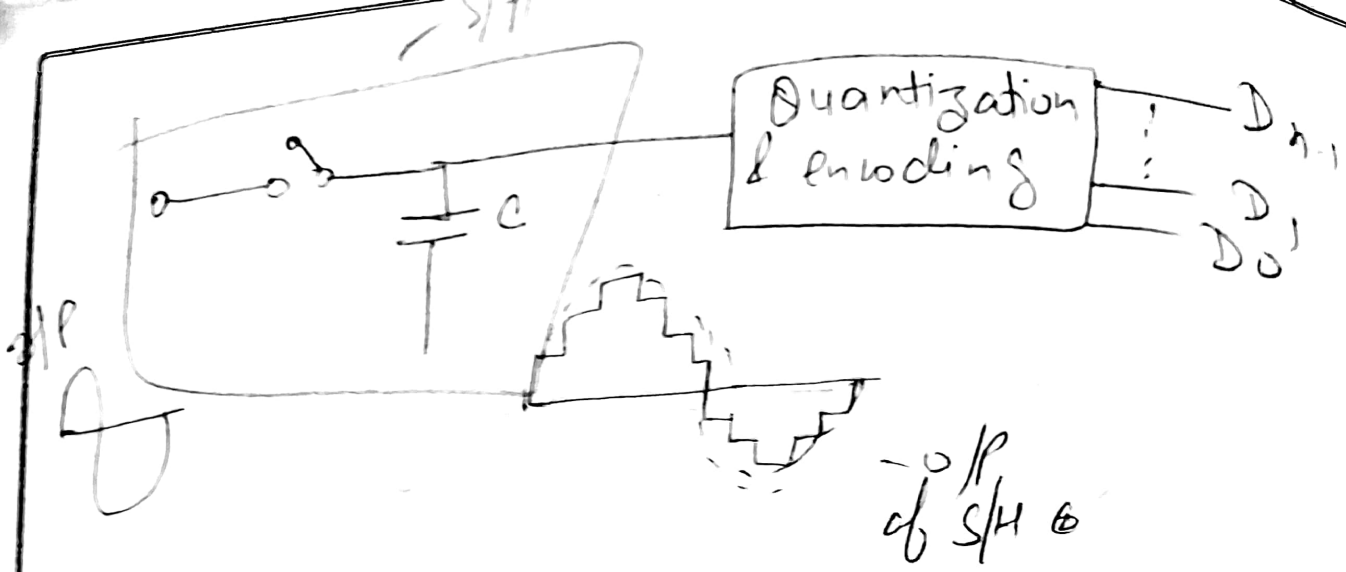
↓

It is the process in which the reference signal is partitioned into several discrete quanta, & then I/P signal is matched with the correct quantum.

↳ Encoding means for each quantum, a unique digital code will be assigned & after that the I/P signal is allocated with this digital code.

For understanding this, we can 1st go through the term Resolution used in ADC. It is the smallest variation in analog signal that will result in a variation in the digital o/p. This actually represents the quantization error.

Teacher's Signature :



$$\text{Resolution}, \Delta V = \frac{V_r}{2^N}$$

V_r = Reference Voltage Range

2^N → No. of States

N → No. of bits in digital o/p

The process of Quantization & encoding Table

Analog Signal			Digital o/p
7.5	7	$7\Delta = 7\Delta$	111
6.5	6	$6\Delta = 6\Delta$	110
4.5	4	$4\Delta = 4\Delta$	100
1.5	1	$1\Delta = 1\Delta$	001
0.5	0	$0\Delta = 0\Delta$	000

Date

Expt. No. _____ Page No. _____

from the Table we observe that only one digital value is used to represent the whole range of voltages in an interval (eg. 4.1 to 4.9 → 4)

Thus an error will occurs & it is called quantization error.

This is the Noise introduced by the process of quantization.

The max. quantization error is

$$\pm \frac{1}{2} \Delta V = \pm 0.5 V$$

Teacher's Signature : _____